APLUS TECHNOLOGY

DDR2-667 UNBUFFERED DIMM 512MB 64x8

DESCRIPTION:

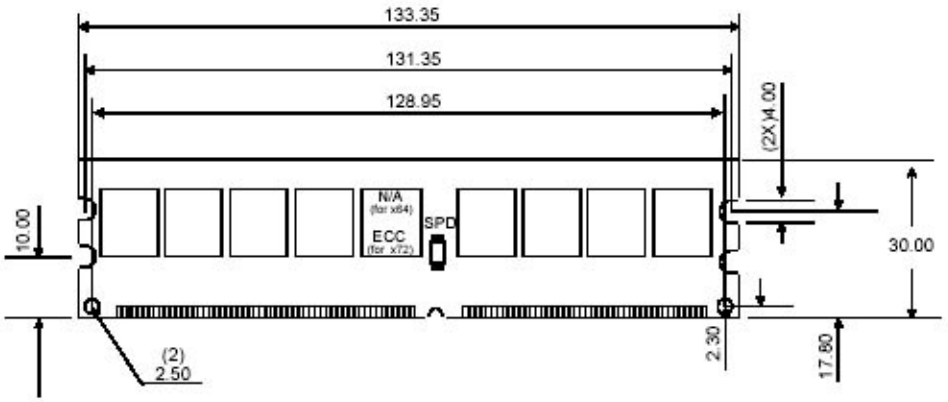
This document describes Aplus 64M x 64-bit 512MB DDR2-667 CL5 SDRAM (Synchronous DRAM) memory module The components on this module include eight 64M x 8-bit (4Banks) DDR2-667 SDRAM in FBGA packages. This 240-pin DIMM uses gold contact fingers and requires +1.8V. The electrical and mechanical specifications are as follows:

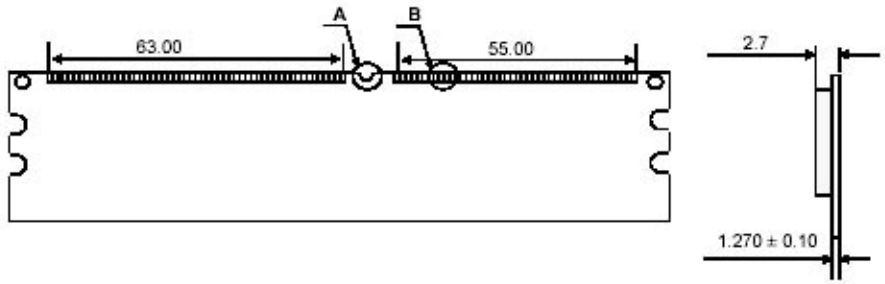
FEATURES:

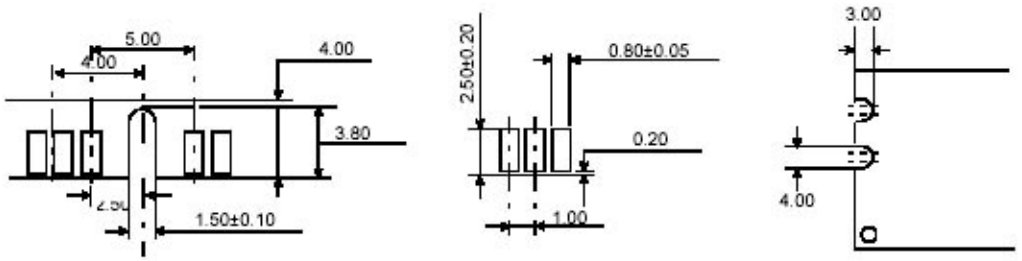
JEDEC standard 1.8V ± 0.1V Power supply
All inputs and outputs SSTL_1.8 compatible
Max clock Freq: 333Mhz
Double-data-rate architecture; two data transfers per clock cycle
Bidirectional data strobe (DQS)
Differential clock inputs (CK and CK)
DLL aligns DQ and DQS transition with CK transition
Programmable Read latency 5 (clock)
Programmable Burst length (4,8)
Programmable Burst type (sequential & interleave)
Timing Reference: CL-tRCD-tRP (5-5-5)
Edge aligned data output, center aligned data input
Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
OCD (Off-chip driver impedance adjustment)
ODT (On-die termination)
Serial presence detect with EEPROM

PERFORMANCE:

Clock Cycle Time (tCK)	3ns (min.) /8ns (max.)
Row Cycle Time (tRC)	54ns (min.)
Refresh Row Cycle Time (tRFC)	105ns (min.)
Row Active Time (tRAS)	39ns (min.) /70,000ns (max.)
Operating Temperature	0℃ ~ 85℃
Storage Temperature	-55℃ ~ +100℃


133.35
131.35
128.95
(2X)4.00
10.00
N/A
(for x64)
ECC
(for x72)
SPD
30.00
(2)
2.50
2.30
17.80


A
B
63.00
55.00
2.7
1.270 ± 0.10


5.00
4.00
4.00
3.80
1.50±0.10
Detail A
2.50±0.20
0.80±0.05
0.20
1.00
Detail B
3.00
4.00