APLUS TECHNOLOGY

# DDR2-533 REGISTERED DIMM 4GB 256x4

## DESCRIPTION:

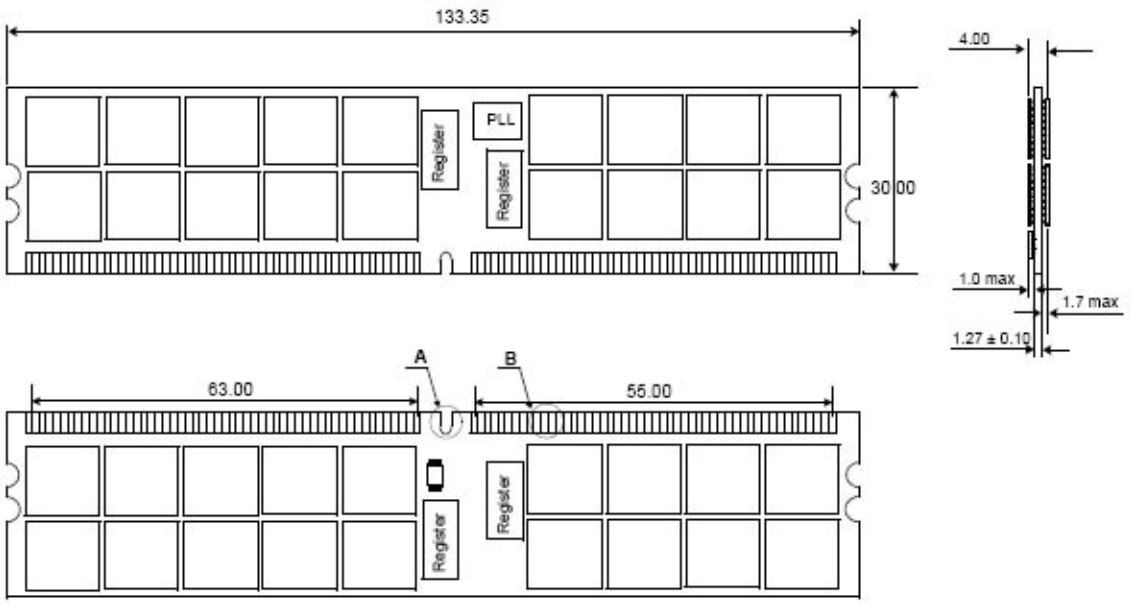
This document describes Aplus 512M x 72-bit 4GB DDR2-533 CL4 SDRAM (Synchronous DRAM) Registered ECC memory module The components on this module include thirty-six 256M x 4-bit (8Banks) DDR2-533 SDRAM in FBGA packages. This 240-pin DIMM uses gold contact fingers and requires +1.8V. The electrical and mechanical specifications are as follows:

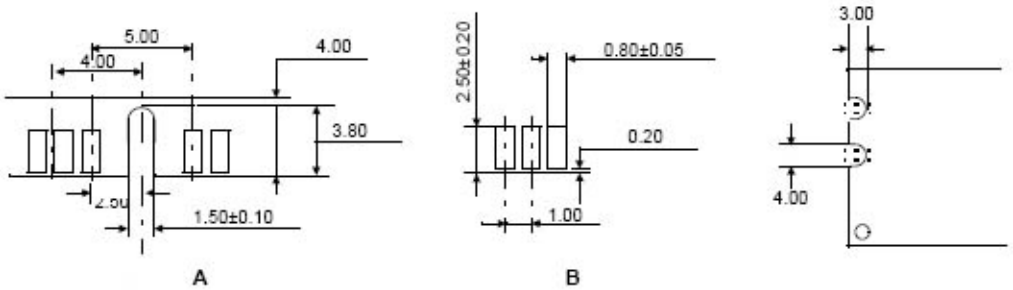
## FEATURES:

JEDEC standard 1.8V ± 0.1V Power supply
All inputs and outputs SSTL_1.8 compatible
Max clock Freq: 267Mhz
Double-data-rate architecture; two data transfers per clock cycle
Bidirectional data strobe (DQS)
Differential clock inputs (CK and CK)
DLL aligns DQ and DQS transition with CK transition
Programmable Read latency 4 (clock)
Programmable Burst length (4,8)
Programmable Burst type (sequential & interleave)
Timing Reference: CL-tRCD-tRP (4-4-4)
Edge aligned data output, center aligned data input
Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
Error Check Correction ( ECC ) Capability
High temperature self-refresh Entry enablble features
PASR ( Partial array self refresh )
OCD ( Off-chip driver impedance adjustment )
ODT ( On-die termination )
Serial presence detect with EEPROM

## PERFORMANCE:

| | |
|---|---|
| Clock Cycle Time ( tCK ) | 5ns (min.) /8ns (max.) |
| Row Cycle Time ( tRC ) | 55ns (min.) |
| Refresh Row Cycle Time ( tRFC ) | 105ns (min.) |
| Row Active Time ( tRAS ) | 40ns (min.) /70,000ns (max.) |
| Operating Temperature | 0℃ ~ 85℃ |
| Storage Temperature | -55℃ ~ +100℃ |


133.35
30.00
Register
PLL
Register
4.00
1.0 max
1.7 max
1.27 ± 0.10
A
B
63.00
55.00
Register
Register


5.00
4.00
4.00
3.80
1.50±0.10
A
2.50±0.20
0.80±0.05
0.20
1.00
B
3.00
4.00