APLUS TECHNOLOGY

DDR2-400 UNBUFFERED ECC DIMM 512MB 64x8

DESCRIPTION:

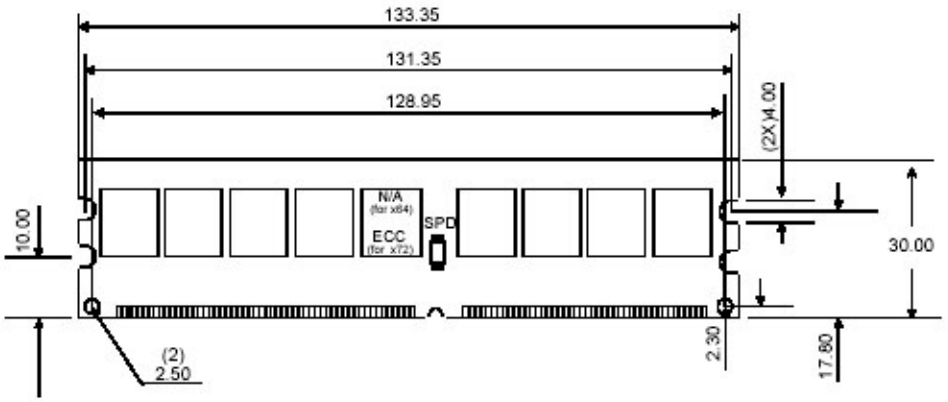
This document describes Aplus 64M x 72-bit 512MB DDR2-400 CL3 SDRAM (Synchronous DRAM) ECC memory module The components on this module include nine 64M x 8-bit (4Banks) DDR2-400 SDRAM in FBGA packages. This 240-pin DIMM uses gold contact fingers and requires +1.8V. The electrical and mechanical specifications are as follows:

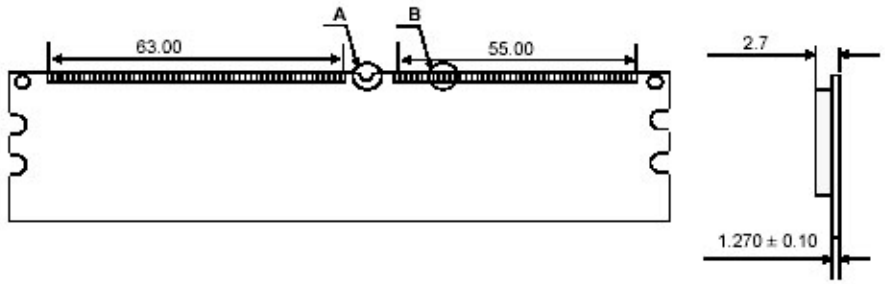
FEATURES:

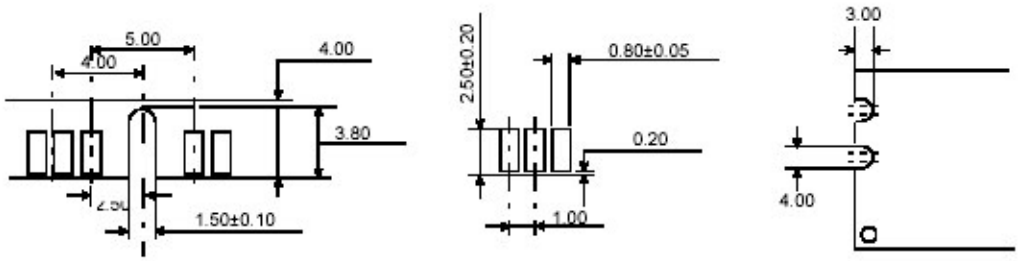
JEDEC standard 1.8V ± 0.1V Power supply
All inputs and outputs SSTL_1.8 compatible
Max clock Freq: 200Mhz
Double-data-rate architecture; two data transfers per clock cycle
Bidirectional data strobe (DQS)
Differential clock inputs (CK and CK)
DLL aligns DQ and DQS transition with CK transition
Programmable Read latency 3 (clock)
Programmable Burst length (4,8)
Programmable Burst type (sequential & interleave)
Timing Reference: CL-tRCD-tRP (3-3-3)
Edge aligned data output, center aligned data input
Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
PASR (Partial array self refresh)
OCD (Off-chip driver impedance adjustment)
ODT (On-die termination)
Serial presence detect with EEPROM

PERFORMANCE:

Clock Cycle Time (tCK)	5ns (min.) /8ns (max.)
Row Cycle Time (tRC)	55ns (min.)
Refresh Row Cycle Time (tRFC)	105ns (min.)
Row Active Time (tRAS)	40ns (min.) /70,000ns (max.)
Operating Temperature	0℃ ~ 85℃
Storage Temperature	-55℃ ~ +100℃







Detail A Detail B