Features

- 100-pin, dual in-line memory module(DIMM)
- Fast data transfer rate: PC2100 and PC2700
- Utilizes 266MT/s or 333MT/s DDR SDRAM components
- 128MB (16 Meg x 32), 256MB (32 Meg x 32), 512MB (64 Meg x 32)
- V_{DD} = +2.5V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/ received with data-*i.e.*, source-synchronous data capture
- Differential clock inputs CK and CK#
- Four internal device banks for concurrent operation
- Programmable burst lengths:2, 4 or 8
- Auto precharge option
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latenct
- Auto Refresh and Self Refresh Modes
- 15.625 μ s(128MB), 7.8125 μ s(256MB, 512MB)maximum average periodic refresh interval
- Gold edge contacts
- Dual rank

Pin Assignment and Descriptions

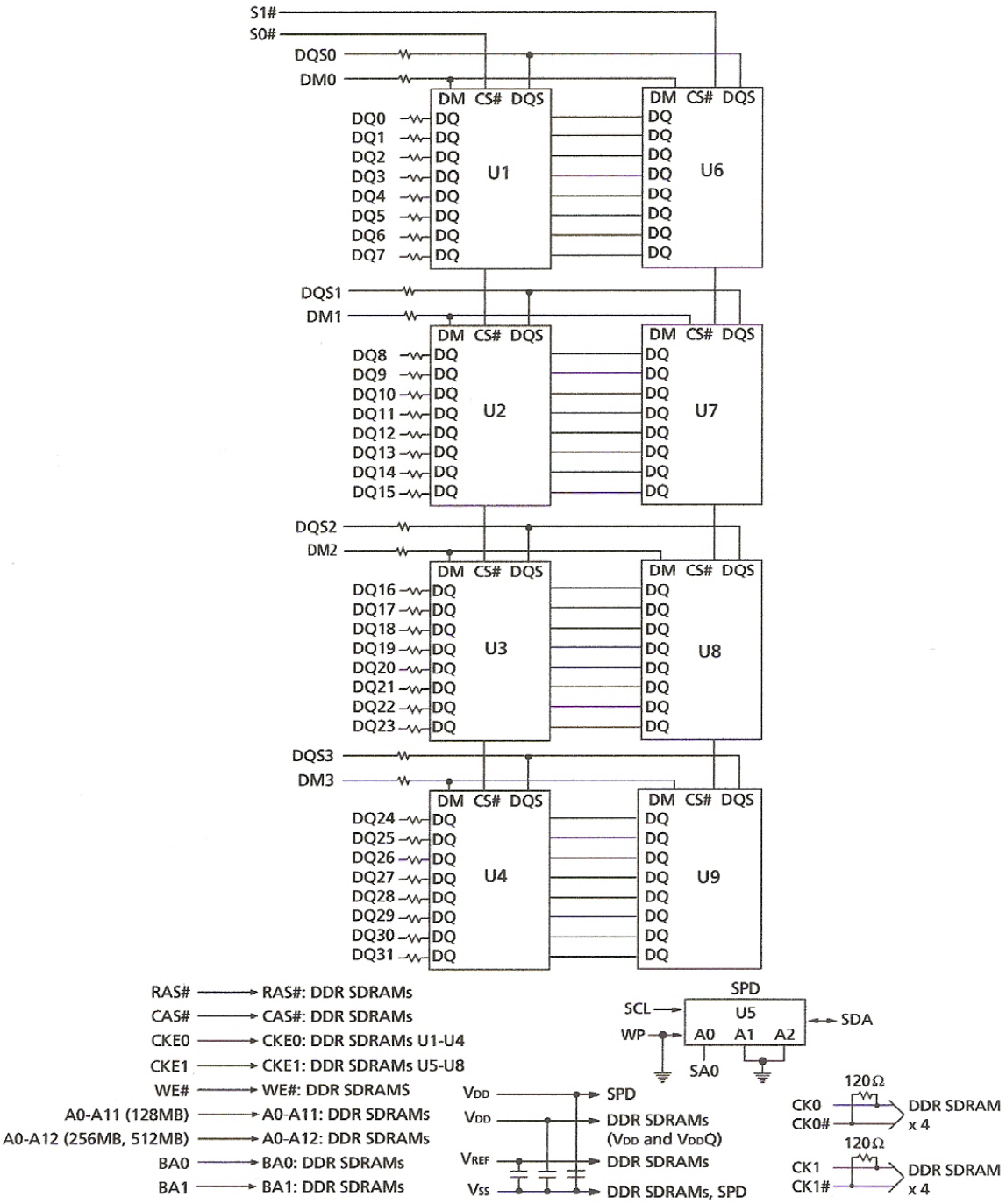
Pin Assignment

100-Pin DIMM Front								100-Pin DIMM Back							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**
1	DQ0	14	V_{DD}	26	A5	39	DQ18	51	DQ4	64	V_{DD}	76	A2	89	DQ22
2	V_{SS}	15	DQ11	27	A3	40	DQ19	52	V_{SS}	65	DQ15	77	A0	90	DQ23
3	DQ1	16	V_{SS}	28	A1	41	V_{DD}	53	DQ5	66	V_{SS}	78	BA1	91	V_{DD}
4	DQS0	17	CK0	29	A10	42	DQ24	54	DM0	67	CK1	79	RAS#	92	DQ28
5	V_{DD}	18	CK0#	30	V_{DD}	43	DQ25	55	V_{DD}	68	CK1#	80	V_{DD}	93	DQ29
6	DQ2	19	V_{DD}	31	BA0	44	V_{SS}	56	DQ6	69	V_{DD}	81	CAS#	94	V_{SS}
7	DQ3	20	CKE1	32	WE#	45	DQS3	57	DQ7	70	CKE0	82	S1#	95	DM3
8	V_{DD}	21	NC/A12	33	S0#	46	DQS6	58	V_{DD}	71	A11	83	DNU	96	DQ30
9	DQ8	22	NC	34	DQ16	47	V_{SS}	59	DQ12	72	A8	84	DQ20	97	V_{SS}
10	DQ9	23	A9	35	V_{SS}	48	DQ27	60	DQ13	73	A6	85	V_{SS}	98	DQ31
11	V_{SS}	24	A7	36	DQ17	49	SA0	61	V_{SS}	74	A4	86	DQ21	99	SDA
12	DQS1	25	V_{SS}	37	DQS2	50	V_{REF}	62	DM1	75	V_{SS}	87	DM2	100	SCL
13	DQ10			38	V_{DD}			63	DQ14			88	V_{DD}		

Functional Block

Standard modules use the following DDR SDRAM devices: 16×8 8chips(128MB); 32×8 8chips(256MB); and 64×8 8chips(512MB).

Functional Block Diagram



Parameter Table

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reli- ability.

Voltage on VDD Supply Relative to VSS . . . . . -1V to +3.6V
Voltage on VREF and Inputs Relative to VSS . . . . . -1V to +3.6V
Voltage on I/O Pins Relative to VSS . . . . -0.5V to VDD +0.5V
Operating Temperature,
T_A (commercial - ambient) . . . . 0°C to +70°C
T_A (industrial - ambient) . . . . -40°C to +85°C
Storage Temperature (plastic) . . . . -55°C to +150°C
Short Circuit Output Current. . . . . … 50mA

DC Electrical Characteristics and Operating Conditions

Notes: 1–5, 14, 48; notes appear on pages 23–27; 0°C ≤ T_A ≤ +70°C

Parameter/Condition		Symbol	Min	Max	Units
Supply Voltage		VDD	2.3	2.7	V
I/O Supply Voltage		VDD	2.3	2.7	V
I/O Reference Voltage		VREF	0.49xVDD	0.51xVDD	V
I/O Termination Voltage (system)		VTT	VREF - .04	VREF+0.04	V
Input High (Logic 1) Voltage		VIH (DC)	VREF+0.15	VDD + 0.3	V
Input Low (Logic 0) Voltage		VIL (DC)	-0.3	VREF -0.15	V
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ VDD, VREF pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	Command/ Address, RAS#, CAS#, WE#	II	-16	16	µA
	CKE0, CKE1, S0#, S1# CK, CK#		-8	8	
	DM		-4	4	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDD)	DQ, DQS	IOZ	-10	10	µA
OUTPUT LEVELS High Current (VOUT = VDD-0.373V, minimum VREF, minimum VTT)		IOH	-16.8	–	mA
Low Current (VOUT = 0.373V, maximum VREF, maximum VTT)		IOL	16.8	–	mA

AC Input Operating Conditions

Notes: 1–5, 14, 48, 49; notes appear on pages 23–27; 0°C ≤ T_A ≤ +70°C; VDD = +2.5V ±0.2V

Parameter/Condition	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	VIH (AC)	VREF + 0.310	–	V
Input Low (Logic 0) Voltage	VIL (AC)	–	VREF - 0.310	V
I/O Reference Voltage	VREF (AC)	0.49 x VDD	0.51 x VDD	V

Module Dimension

All dimensions are in inches (millimeters); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

100-Pin DIMM Dimensions