APLUS TECHNOLOGY

DDRII SDRAM 800/667/533 144-PIN SO_DIMM 1GB 128Mx8

DESCRIPTION:

This document describes Aplus 128M x 32-bit 1GB DDR2-800/667/533 SDRAM (Synchronous DRAM) Memory Module. The components on this module include eight 128M x 8-bit (8 Banks) DDR2-800/667/533 SDRAMs in FBGA packages This 144-pin SO-DIMM is used gold contact fingers and requires +1.8V. The electrical and mechanical specifications are as follows:

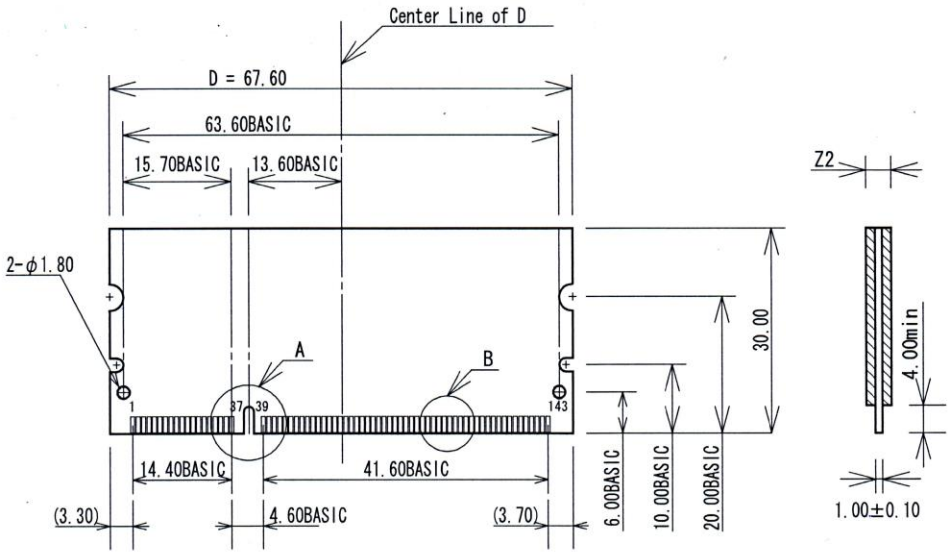
Features

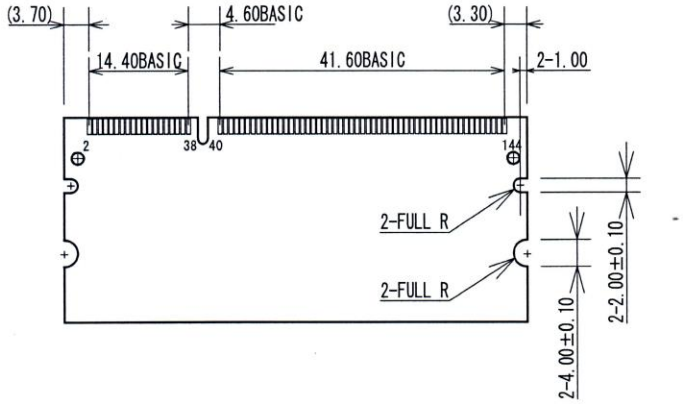
JEDEC standard 1.8V±0.1V Power supply
All inputs and outputs SSTL_1.8 compatible
Max clock Freq: 400Mhz ,333Mhz ,267Mhz
Double-data-rate architecture; two data transfers per clock cycle
Bidirectional data strobe(DQS)
Differential clock inputs (CK and CK)
DLL aligns DQ and DQS transition with CK transition
Programmable Read latency 5 (clock)
Programmable Burst length (4,8)
Programmable Burst type (sequential & interleave)
Timing Reference; CL-tRCD-tRP(5-5-5) ,(4-4-4)
Edge aligned data output, center aligned data input
Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
OCD (Off-chip driver impedance adjustmant)
ODT (On-die termination)
Serial presence detect with EEPROM

PERFORMANCE

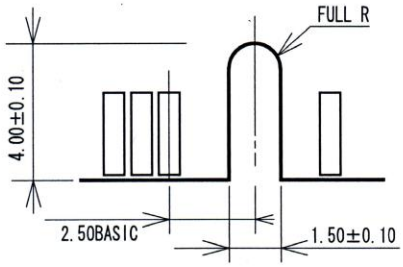
Clock Cycle Time (tCK)	2.5ns (min.) /8ns (max.)
Row Cycle Time (tRC)	51.5ns (min.) , 54ns (min.) , 55ns (min.)
Refresh ROW Cycle Time (tREC)	105ns (min.)
Row Active (tRAS)	39ns (min.) /70,000ns (max.) , 40ns (min.) /70,000ns (max.)
Operating Temperature	0℃~85℃
Storage Temperature	-55℃~+100℃

144-Pin DDR2 SODIMM

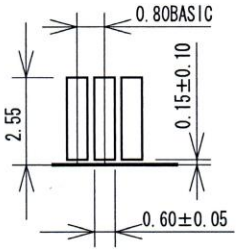




Detail A



Detail B



Unit: mm
Tolerance: ±0.15mm
Except V-cut area